Integration of the General Network Theorem in ADE and ADE XL: Toward a Deeper Insight Into Circuit Behavior

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Presented is the integration of the General Network Theorem (GNT) and its descendants, General Feedback Theorem (GFT), Extra Element Theorem (EET) and Chain Theorem (CT) as an analysis in ADE (XL) [1,2,3]. In contrast with our previous implementation [5], the new approach fully integrates with ADE and ADE XL. These analyses are extensively used both in real tape-out designs and introduced to students along with Virtuoso. In this way, combined with theoretical treatment and simple hand calculations, they develop a deeper understanding of the examined circuit. Also, given the complexity of modern circuits and devices, they learn how to quickly develop useful analytical approximations, apply them to further design, all within the Virtuoso environment.

Introduction and Motivation of Work

In circuit design and in teaching, various small-signal analyses are used to verify linear circuit behavior. Rather than examining full-blown transfer functions from input to output, additional insight can be gained by using several simpler lower-level transfer functions, each portraying a subset of the circuit properties—a divide-and-conquer approach. The General Network Theorem (GNT), having a solid theoretical foundation, provides exact solutions for these lower-level transfer functions for any linear circuit, however complex. They are calculated by injecting one or more voltage or current test signals. The injection configuration determines the resulting decomposition. Depending on the test signal injection configuration, the GNT morphs into the General Feedback Theorem (GFT), (N-) Extra Element Theorem (N-EET) or chain theorem (CT).

The GNT states *how* to analytically calculate the lower-level transfer functions in an insightful manner: using injection and nulling calculations [1], the results naturally appear in low-entropy factored pole-zero form, which are useful for design. This decomposition of a potentially complex transfer function in simpler parts is highly desirable, as it often leads to additional insight into circuit behavior and provides better design guidance.

We have integrated the GNT as an analysis in Virtuoso's ADE and ADE XL to allow direct application of the theorem to real-world design. It allows validating hand analysis results (a posteriori) or finding out which lower-level transfer function dominate circuit behavior (a priori). In addition, introducing it to students along with Virtuoso helps them to quickly grasp more advanced circuit concepts and appreciate the sources of discrepancies between theoretical results and practical implementations. The GNT framework also allows one to retain overview in complex circuits and the same calculation techniques are applied to different situations. In additions, well-known results such as Blackman's formula and the various feedback relations all derive cleanly from the GNT. With this tool, validation of the theory in Virtuoso is easily accomplished.

Overview of the General Network Theorem

The General Network Theorem or Dissection Theorem [1] states that any transfer function of a linear circuit H can be decomposed into lower-level transfer functions, which are found by injecting a single test signal:

$$H = H_{\infty} \frac{1 + 1/T_n}{1 + 1/T} = H_{\infty} \frac{T}{1 + T} + H_0 \frac{1}{1 + T}$$

By injecting multiple test signals T, Tn and H0 can further be factored. Depending on the test signal injection configuration, the GNT morphs into the GFT, N-EET or CT, in which the lower-level transfer functions have a particular interpretation.

As the GFT, Hinf represents the 'ideal', desired transfer function with infinite loop gain. T is the loop gain and Tn the null loop gain. H0 exhibits the direct forward transmission, which is important when the loop gain becomes small. Their values are obtained by injecting both a voltage and a current such that the total feedback error signal is nulled. The loop gain consist of a forward and reverse contribution (Tfwd and Trev), both of which are the parallel combination of a part due to voltage injection and part due to current injection [1]. The null loop gain is factored in a similar way.

The GNT used as GFT differs from Spectre's stb analysis' [6] as not only loop gain is considered. Indeed, a detailed factorization of the closed loop transfer function is calculated. Also, stb's loop gain is defined as Tfwd + Trev, whereas GFT's loop gain, as derived from the GNT, is Tfwd/(1+Trev). In practical circuits, however, Trev is usually small.

In the N-EET interpretation, a transfer function is expressed in terms of its value when *N* given extra elements (EEs) are absent (Hinf), and a correction factor involving the EEs and the (null) driving point impedances seen by the elements. An EE is made absent by replacing it with either zero or infinite impedance [4].

When used as CT, the GNT analysis factors a transfer function such that the loading effect of a stage on the previous one becomes clear [2].

Integration in Virtuoso

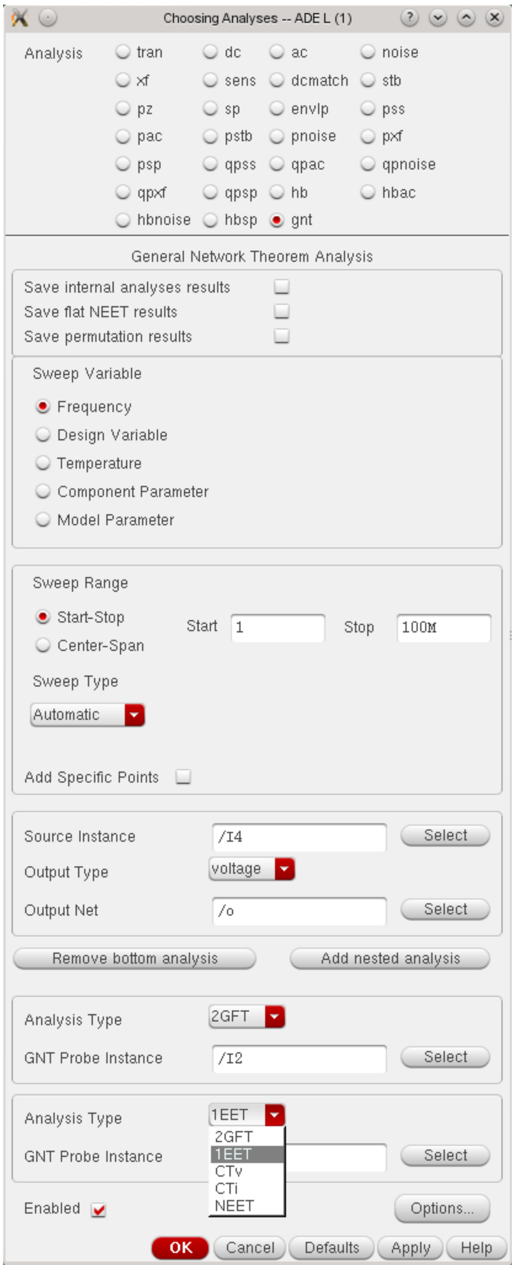


Figure 1: gnt analysis form

Our GNT implementation in ADE (XL) aims to be fully transparent with use model identical to the other analysis types, in contrast with our previous work [5]. As shown in Figure 1, the GNT integrates with the familiar *Choosing Analyses* form for Spectre/APS and presents options similar to ac, stb and the like. This implementation supports nested GNT analyses, such as doing an EET analysis on the lower-level transfer functions of a GFT factorization.

The user selects the desired variable over which to sweep and sets the sweep range and sweep type. A source instance and output net (for voltage output) or output probe (for current output) are required to define which transfer function is to be decomposed. For each level of nesting, one or more *GNTProbe* instances are selected as well as the desired GNT analysis type (GFT, CT or N-EET). The probes are placed by the user at the correct error signal injection point for the selected analysis. They provide the means for injecting a voltage and/or current in an internal AC analysis. The probes are transparent to other analyses, Layout XL and Calibre LVS tools. Further simulation options are available under the *Options…* button. Internally the results are calculated as a single flat N-EET, whether or not the analyses are nested. The user can optionally save the raw N-EET data as well as the results of any possible permutation of the given nested analyses order, which are readily available in the flat N-EET solution.

The decomposition results are included in the psf data and can be accessed with ViVa's Results Browser, as depicted in Figure 2. Results of nested analyses are available in folders. Parametric sweeps in ADE L can be used. ADE XL support includes corners, parameters, Monte Carlo sampling, sensitivity analysis, optimization, worst-case corners, a.o.. In addition, the getData() SKILL API is supported, allowing scripted post-processing.

The integration has been tested on IC 6.1.5 and IC 6.1.6.

Application examples

This section will demonstrate the use of the GNT analysis and its descendants based on an example that could serve as an assignment during an electronics course. An on-chip voltage regulator is designed and its behavior is verified. Consider the schematic in Figure 3: a folded cascode OTA and emitter follower in unity-gain feedback configuration.

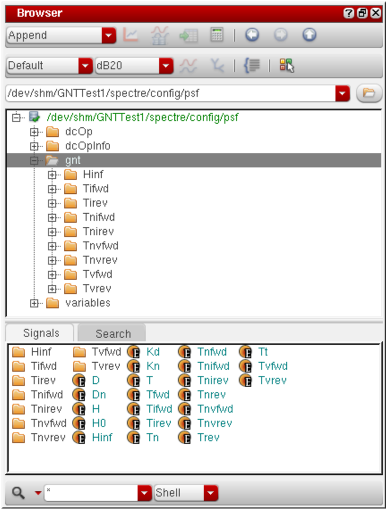


Figure 2: gnt analysis results in the Results Browser

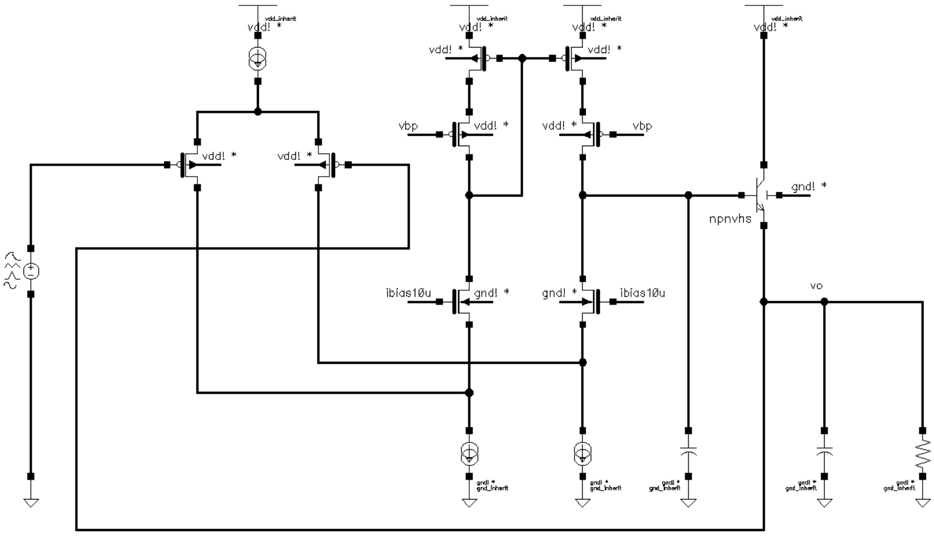


Figure 3: voltage regulator circuit

After the initial design phase, the output voltage accuracy is found to be insufficient. As this is a feedback system, the GFT variant of the GNT can provide some insight. A GNT probe is placed at the error signal of the loop (Figure 5a) and a GFT analysis, using this probe, is run. Figure 4a shows selected results of the analysis. Ideally, the output voltage should follow the input, but H is only -2.5 dB at low frequencies, which explains the low accuracy in this case. As Hinf is exactly 0 dB and H0 is negligible (not shown), the cause must be insufficient loop gain. Indeed, the DC loop gain is only 10 dB, way too low to obtain a reasonable accuracy and much lower than expected from a folded cascode OTA. Furthermore, it is recognized that the loop gain can be approximated by Tvfwd, one of T's components.

To capture the loading effect of the follower on the OTA, a second GNT probe is placed between the stages (Figure 5b). To explore the issue with Tvfwd further, a nested analysis is performed, in which the CT analysis is applied to the GFT results using the newly placed probe. Figure 4b shows selected results. Tvfwd.Hinf is the loop gain without loading effect and is much higher than the actual loop gain. This indicates excessive interaction between the two stages.

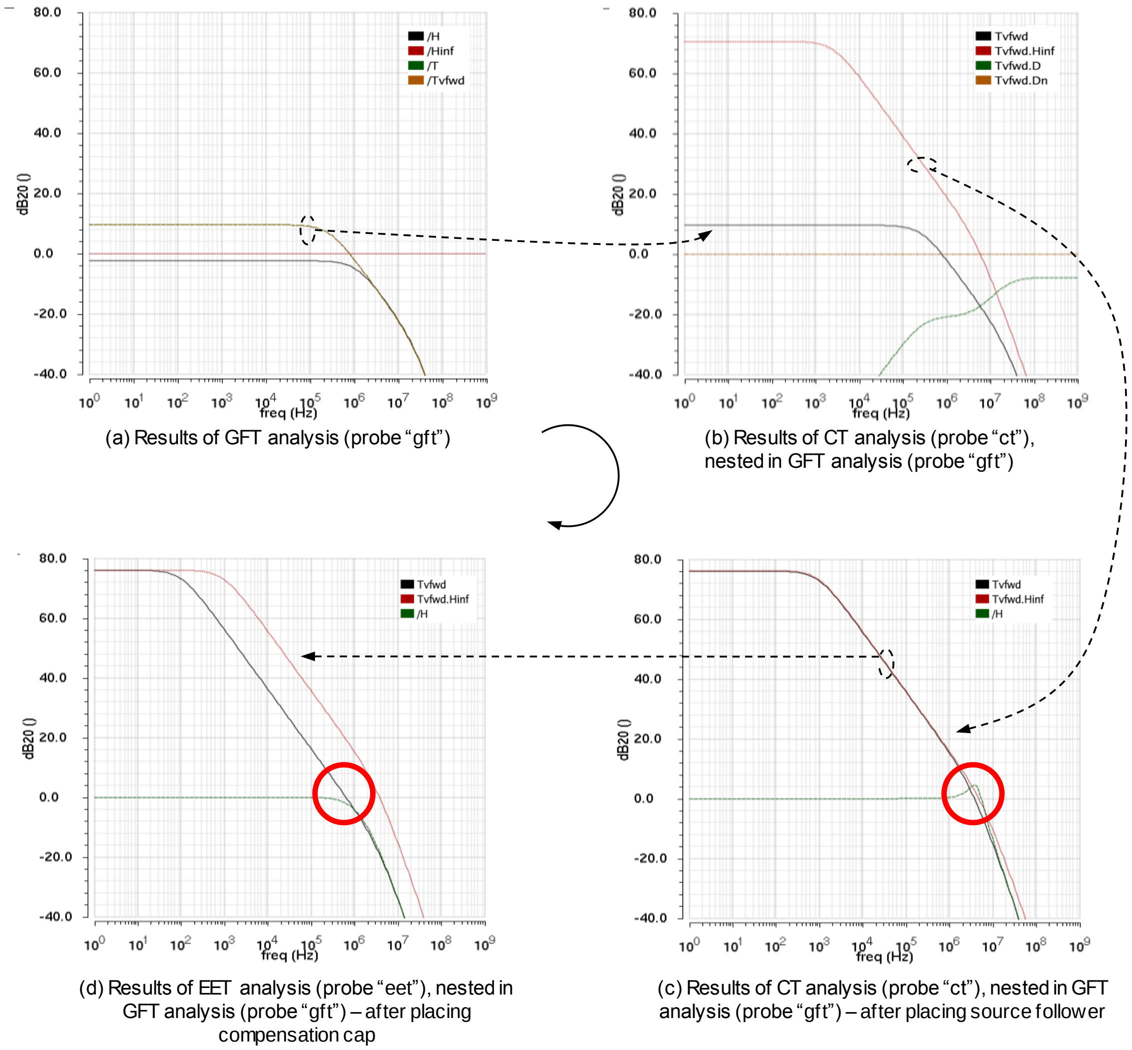
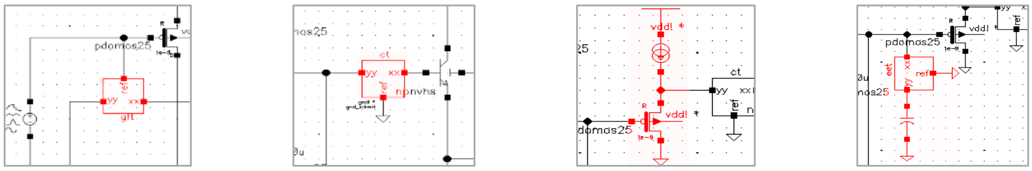


Figure 4: results of consecutive GNT analyses

A possible solution could be to insert a buffer between both stages. Figure 5c shows the inclusion of a PMOS source follower. A re-run of the previous analysis gives the results shown in Figure 4c. Clearly, the DC loop gain has improved, resulting in a closed-loop DC gain of -1.6 mdB. The output will now accurately follow the input. However, some peaking can now be observed in H. This peaking is caused by insufficient phase margin, currently at 35°. The loop will now be compensated by adding capacitance to the output of the folded cascode to ground (Figure 5d). The effect of this modification on the loop gain is exposed by nesting the EET—using the probe shown in Figure 5d—inside the GFT, the results of which are shown in Figure 4d. The phase margin has increased to 78° and the closed-loop peaking has disappeared.



(a) Placement of probe "gft" (b) Placement of probe "ct" (c) Placement of source follower (d) Placement of compensation cap, probe "eet"

Figure 5: GNT probe placement and circuit modifications

Conclusion

We have successfully integrated the GNT as an analysis in ADE (XL) with use model identical to existing analyses. This tool allows direct application of the theory in Virtuoso. Hence, it is a helpful instrument for design and analysis of electronic circuits and education of future designers. Using a linear regulator as an example, it was shown how to use the analysis in Virtuoso and how the results lead to increased insight and design guidance in general.

Acknowledgement

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